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BOARD CHARACTERIZATION

ABRACON P/N: ABS06-32.768kHz
Report #170

Presented to:

Atmel

Attention:

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Abracon:

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1 ABSTRACT

3 different customer board designs were received. The 3 boards were subjected to several different types of tests to evaluate the board parameters with ABS06-32.768kHz crystal.

2 TEST EQUIPMENT

TDS 2024B Tektronix Digital Storage Oscilloscope
HP53131A Frequency counter
P2220 Tektronix Passive probe (10X)
1103 Tektronix Probe power supply
TCPA300 Tektronix Current probe amplifier

250B S&A Crystal Impedance tester
TCP312 Tektronix Current probe
E3640 Agilent DC Power supply
E34401A Agilent Digital Multimeter

3 MATERIALS

Boards :
Chipset :
ABRACON Crystal: ABS06-32.768kHz

4 BOARD PHOTO



Design 1: Atmega16/32



Design 2: Atmega64/128/169



Design 3: Atmega164P/324P

5 SPECIFICATION

Frequency:

32.768kHz

Operating temperature:

- 40° C to + 85°C

Turn-over temperature:

+25° C \pm 5° C

Storage temperature:

- 55° C to + 125°C

Frequency tolerance:

\pm 20 ppm max.

Frequency vs. Temperature:

- 0.034 \pm 0.005ppm/°C²

Equivalent series resistance:

90 kohms max.

Load capacitance CL:

12.5 pF

Drive level:

0.5 μ W max.

Aging @ 25° C first year:

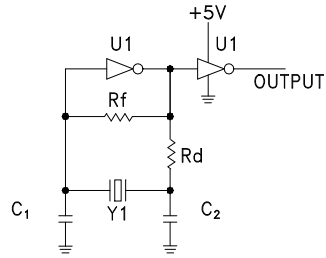
\pm 3 ppm max.

Insulation resistance:

500Mohms with 100Vdc \pm 15V

6 THEORY

6.1 Circuits



U1: ASIC
Y1: CRYSTAL
C₁ C₂: LOAD CAPACITANCE

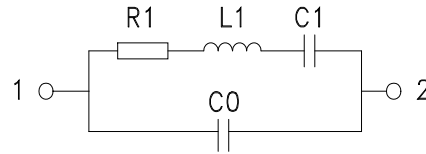


Figure 1B

6.2 Feedback resistor

The feedback resistor Rf sets the DC bias of the inverter at half the Vdd point and value must be chosen to assure the optimal condition at oscillation start-up. Rf is internal to the IC.

6.3 Resonator Y1 and external load capacitance C1, C2

A crystal or ceramic resonator has the equivalent circuit as shown in Figure 1B. The motional and shunt parameters vary with crystal or ceramic resonator and frequency. C0 represents the crystal shunt capacitance. In PCB, we have to add additional stray capacitance that may be present across the crystal terminals (Cso) and between each terminal to ground (Cs1 and Cs2).

6.4 Safety Factor (SF)

Depending on the drive level, the impedance of the crystal changes. The safety factor gives an idea of how much the resistance of the passive part of the oscillator circuitry can be increased. The safety factor is the relationship between maximum negative resistance {-Rv} which can be added in series with the crystal but still oscillating, and the maximum load resonance resistance {ESRmax}.

$$\text{Safety Factor SF} = \{-R_{v\max.}\} / \{ESR_{\max.}\}$$

Qualification of the safety factor:

Safety Factor	Qualification
SF < 1.5	Unacceptable
1.5 ≤ SF < 2	Very Risky
2 ≤ SF < 3	Unreliable
3 ≤ SF < 5	Reliable
SF ≥ 5	Very Reliable

6.5 Drive level

The drive level is mainly controlled via Rd, but also C1 and C2 have an influence.

This particular design does not have Rd. Therefore the drive level will be determined by C1, and C2.

ABRACON recommends keeping the drive level being the typical value and sufficient oscillation margin.

7 BOARD AND CRYSTAL TESTING

7.1 Crystal testing

S&A 250B: 10.07 Report: 4.62

Description: **ABS06-32.768kHz**

Reference Fr: **32.768kHz**

(Using Measured FL)

Crystal	Load Cap	FL	C0	ESR	C1
		ppm	pF	ohms	fF
1	12.5	0.7	1.9	59680.4	6.3

7.2 Optimization of the circuit parameters

7.2.1 Frequency of the board (Original Condition: No external capacitors)

All 3 boards were powered up at 5.5V and measured using 10X passive probe

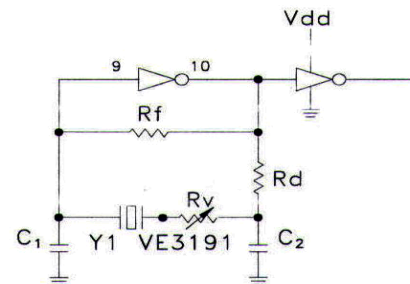
Design	F (Hz)	dF/F (ppm)	Vp-p (V)
Atmega16/32	32,764.803	-97.6	0.668
Atmega64/128/169	32,772.301	131.3	0.408
Atmega164P/324P	32,764.579	-104.4	0.67

7.2.2 Board Evaluation

(Negative Resistance)

Design	-Rv (kΩ)	Safety factor	ESR(kΩ)
Atmega16/32	143	1.6	Very Risky
Atmega64/128/169	805	8.9	Very Reliable
Atmega164P/324P	158	1.8	Very Risky

Please note that, for -R test, the probe was connected to TOSC1/XTAL1 pin. A potentiometer was connected with the crystal in series. Tune the potentiometer until the oscillation stops (no output on the frequency counter). It was found that when the oscillation appeared to have stopped at the crystal pin, if connecting the probe to the "PD7" pin, there was still stable output on pin "PD7".



(Drive level Test)

Design	DL (μW)
Atmega16/32	1.380
Atmega64/128/169	0.936
Atmega164P/324P	0.578

Recommended DL is less than 0.5μW.

There are no external capacitors available to optimize the design for frequency, and possibly drive level / safety margin. It appears that the capacitors are internal to the IC selected for these designs.

